

Product Specification

(Preliminary)

Part Name: OEL Display Module

Customer Part ID:

WiseChip Part ID: UG-2864ASWPG01

Doc No.: SAS1-090BH-A

Customer:
Approved by

CONFIDENTIAL

From: WiseChip Semiconductor Inc.
Approved by

WiseChip Semiconductor Inc.

8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.



Revised History

Part Number	Revision	Revision Content	Revised on
UG-2864ASWPG01	A	New	June 6, 2012
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Contents

Revision History..... *i*

Contents..... *ii*

1. Basic Specifications..... **1~5**

 1.1 Display Specifications 1

 1.2 Mechanical Specifications..... 1

 1.3 Active Area / Memory Mapping & Pixel Construction 1

 1.4 Mechanical Drawing..... 2

 1.5 Pin Definition 3

 1.6 Block Diagram..... 5

2. Absolute Maximum Ratings **6**

3. Optics & Electrical Characteristics **7~11**

 3.1 Optics Characteristics..... 7

 3.2 DC Characteristics 7

 3.3 AC Characteristics..... 8

 3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics..... 8

 3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics..... 9

 3.3.3 Serial Interface Timing Characteristics..... 10

 3.3.4 I²C Interface Timing Characteristics 11

4. Functional Specification..... **12~14**

 4.1 Commands 12

 4.2 Power down and Power up Sequence..... 12

 4.2.1 Power up Sequence 12

 4.2.2 Power down Sequence..... 12

 4.3 Reset Circuit 12

 4.4 Actual Application Example..... 13

5. Reliability **15**

 5.1 Contents of Reliability Tests 15

 5.2 Failure Check Standard 15

6. Outgoing Quality Control Specifications..... **16~19**

 6.1 Environment Required 16

 6.2 Sampling Plan 16

 6.3 Criteria & Acceptable Quality Level..... 16

 6.3.1 Cosmetic Check (Display Off) in Non-Active Area..... 16

 6.3.2 Cosmetic Check (Display Off) in Active Area..... 18

 6.3.3 Pattern Check (Display On) in Active Area..... 19

7. Package Specifications..... **20**

8. Precautions When Using These OEL Display Modules **21~23**

 8.1 Handling Precautions 21

 8.2 Storage Precautions..... 21

 8.3 Designing Precautions..... 22

 8.4 Precautions when disposing of the OEL display modules 22

 8.5 Other Precautions..... 22

Warranty..... **23**

Notice..... **23**

1. Basic Specifications

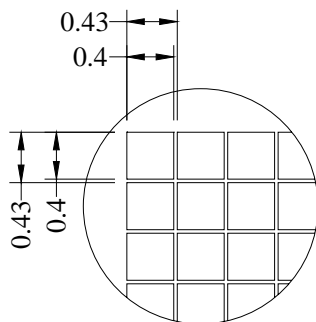
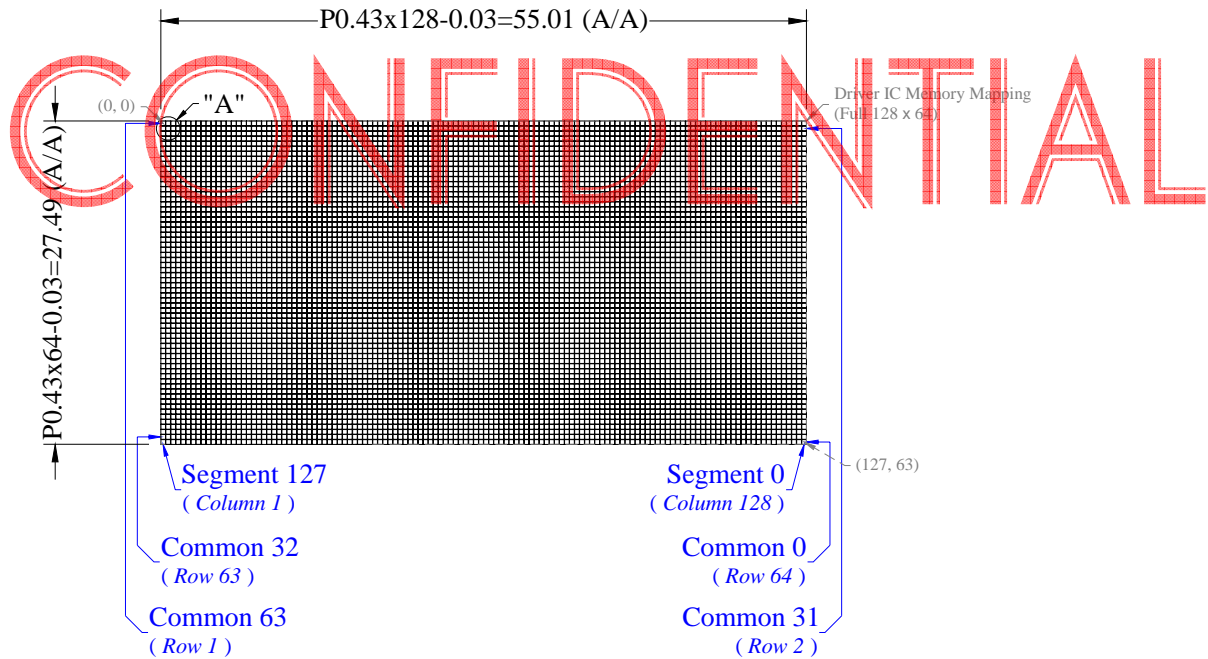
1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: Monochrome (White)
- 3) Drive Duty: 1/64 Duty

1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing
- 2) Number of Pixels: 128 × 64
- 3) Panel Size: 60.50 × 37.00 × 2.00 (mm)
- 4) Active Area: 55.01 × 27.49 (mm)
- 5) Pixel Pitch: 0.43 × 0.43 (mm)
- 6) Pixel Size: 0.40 × 0.40 (mm)
- 7) Weight: 8.60 (g)

1.3 Active Area / Memory Mapping & Pixel Construction



Detail "A"
Scale (10:1)

1.4 Mechanical Drawing

Item A	Date 20120531	Remark Original Drawing
-----------	------------------	----------------------------

Active Area 2.42" 128 x 64 Pixels

Labels: Segment 0 (Column 28), Common 0 (Row 1), Segment 31 (Column 2), Common 31 (Row 2), Segment 127 (Column 128), Common 128 (Row 128).

Detail "A"
Scale (10:1)

Remove Tape t=0.15mm Max
Polarizer t=0.2mm
Glue
Protective Tape 158X3X0.05mm
Contact Side
0.3±0.05

4.5±0.5 (Spacer)
0.4±0.05

(4.35) (34) (1.35) (2.3)

Pin	Symbol	Material	Drawing Number	Rev.
2	VLSR	Soda Lime / Polyimide	DMX2864CNGFBH	A
3	VSS			
4	VDD			
6	BS1			
7	BS2			
9	BS3P			
10	DCA			
11	DVA			
13	DA			
14	D1			
15	D2			
16	D3			
17	D4			
18	D5			
20	D7			
31	UBP			
32	VDDP			
33	VSSP			
34	NC			

Customer Approval Signature

WiseChip Semiconductor Inc.

Unless Otherwise Specified
Unit: mm
General Tolerances:

Dimension: ±0.3
Angle: ±1

Title: UG-2864ASWPG01 Folding Type OEL Display Module
Pixel Number: 128 x 64, Monochrome, COG Package

Drawn: Dora Yang
E.E.: Ting-Kuo Hu
Panel / E.: Ivy Lo
P. M.: Tiffany Hsu

By: 20120531
Date: 20120531
Sheet: 1 of 1
Size: A3

Notes:

1. Color: White
2. Driver IC: SSD1309
3. FPC Number: UT-0205-P05
4. Interface: 8-bit 68XX/80XX Parallel, 4-wire SPI, I2C
5. General Tolerance: ±0.30
6. The total thickness (2.10 Max) is without polarizer protective film & remove tape. The actual assembled total thickness with above materials should be 2.35 Max.

Remove Tape t=0.15mm Max
Polarizer t=0.2mm
Glue
Protective Tape 158X3X0.05mm
Contact Side
0.3±0.05

The drawing contained herein is the exclusive property of WiseChip. It is not allowed to copy, reproduce and/or disclose in any form without permission of WiseChip.

1.5 Pin Definition

Pin Number	Symbol	I/O	Function															
Power Supply																		
5	VDD	P	Power Supply for Logic Circuit This is a voltage supply pin. It must be connected to external source.															
3	VSS	P	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.															
23	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be supplied externally.															
2	VLSS	P	Ground of Analog Circuit This is an analog ground pin. It should be connected to V _{SS} externally.															
Driver																		
21	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and V _{SS} . Set the current at 10μA.															
22	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V _{SS} .															
Interface																		
6 7	BS1 BS2	I	<p>Communicating Protocol Select These pins are MCU interface selection input. See the following table:</p> <table border="1"> <thead> <tr> <th></th> <th>BS1</th> <th>BS2</th> </tr> </thead> <tbody> <tr> <td>I²C</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire Serial</td> <td>0</td> <td>0</td> </tr> <tr> <td>8-bit 68XX Parallel</td> <td>0</td> <td>1</td> </tr> <tr> <td>8-bit 80XX Parallel</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		BS1	BS2	I ² C	1	0	4-wire Serial	0	0	8-bit 68XX Parallel	0	1	8-bit 80XX Parallel	1	1
	BS1	BS2																
I ² C	1	0																
4-wire Serial	0	0																
8-bit 68XX Parallel	0	1																
8-bit 80XX Parallel	1	1																
9	RES#	I	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.															
8	CS#	I	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.															
10	D/C#	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I ² C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
12	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{SS} .															
11	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{SS} .															

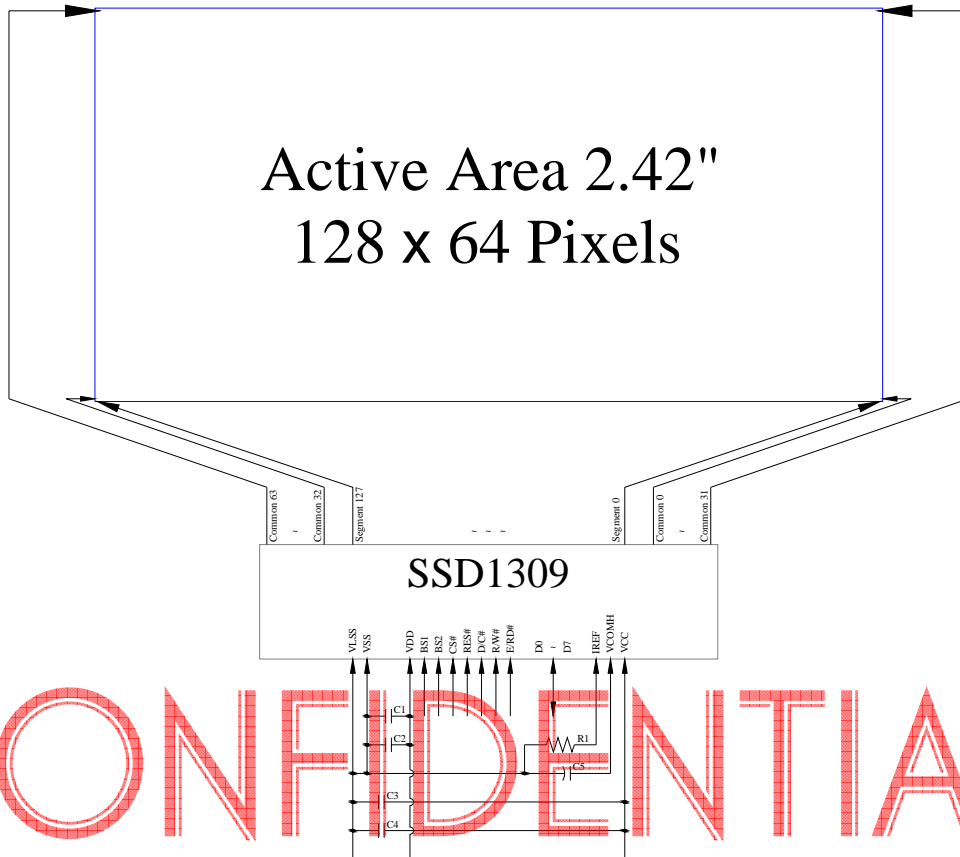
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1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
<i>Interface (Continued)</i>			
13~20	D0~D7	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I ² C mode is selected, D2, D1 should be tied together and serve as SDA _{OUT} , SDA _{IN} in application and D0 is the serial clock input, SCL. Unused pins must be connected to V _{SS} except for D2 in serial mode.
<i>Reserve</i>			
4	N.C.	-	Reserved Pin The N.C. pin between function pins is reserved for compatible and flexible design.
1, 24	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

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1.6 Block Diagram



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MCU Interface Selection: BS1 and BS2
 Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES#, and CS#

- C1, C3: 0.1μF
- C2: 4.7μF
- C4: 10μF
- C5: 4.7μF / 25V Tantalum Capacitor
- R1: 910kΩ, R1 = (Voltage at IREF - BGGND) / IREF

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (80 cd/m ²)		30,000	-	hour	4
Life Time (60 cd/m ²)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of " $V_{SS} = 0V$ ".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: $V_{CC} = 13.0V$, $T_a = 25^\circ C$, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

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3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	60	80	-	cd/m ²
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at $V_{DD} = 2.8V$, $V_{CC} = 13.0V$.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 5	12.5	13.0	13.5	V
High Level Input	V_{IH}	$I_{OUT} = 100\mu A$, 3.3MHz	$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	$I_{OUT} = 100\mu A$, 3.3MHz	0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OH}	$I_{OUT} = 100\mu A$, 3.3MHz	$0.9 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	$I_{OUT} = 100\mu A$, 3.3MHz	0	-	$0.1 \times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC}	I_{CC}	Note 6	-	18.5	23.1	mA
		Note 7	-	27.1	33.9	mA
		Note 8	-	42.3	52.9	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 6: $V_{DD} = 2.8V$, $V_{CC} = 13.0V$, 30% Display Area Turn on.

Note 7: $V_{DD} = 2.8V$, $V_{CC} = 13.0V$, 50% Display Area Turn on.

Note 8: $V_{DD} = 2.8V$, $V_{CC} = 13.0V$, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

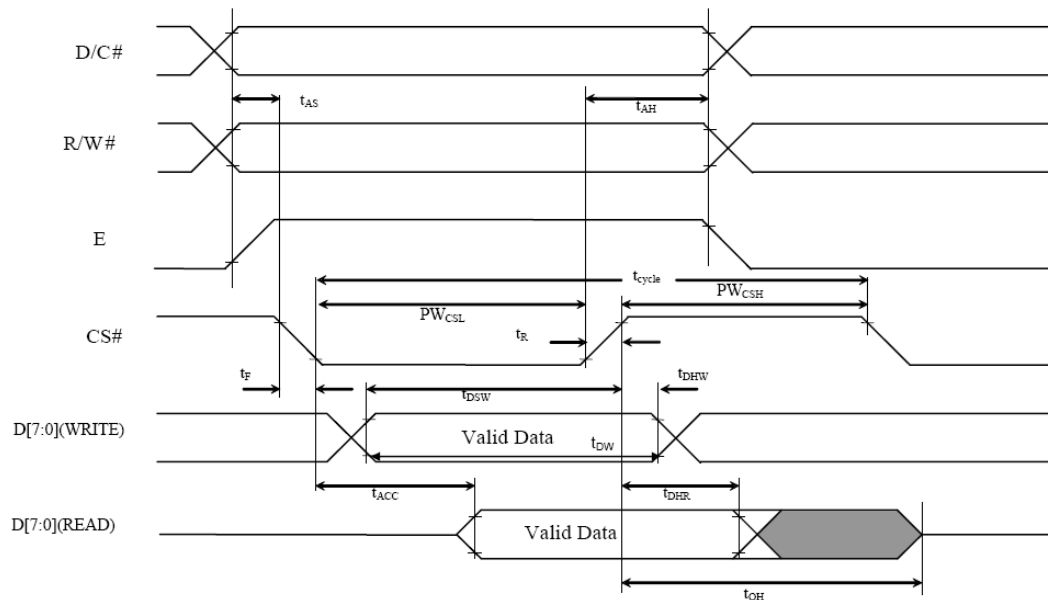
3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	80	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_r	Rise Time	-	40	ns
t_f	Fall Time	-	40	ns

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* ($V_{DD} - V_{SS} = 1.65V$ to $3.3V$, $T_a = 25^\circ C$)

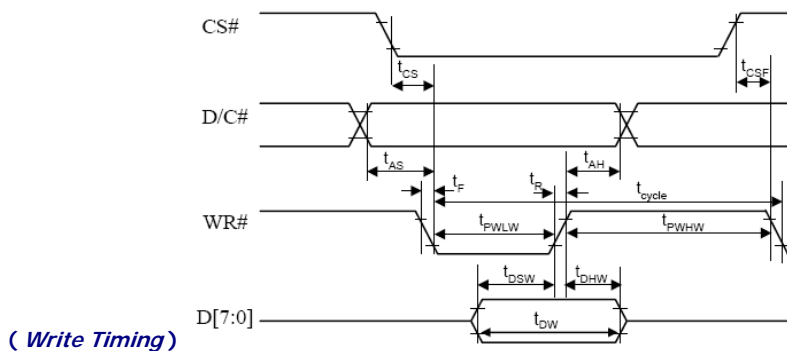
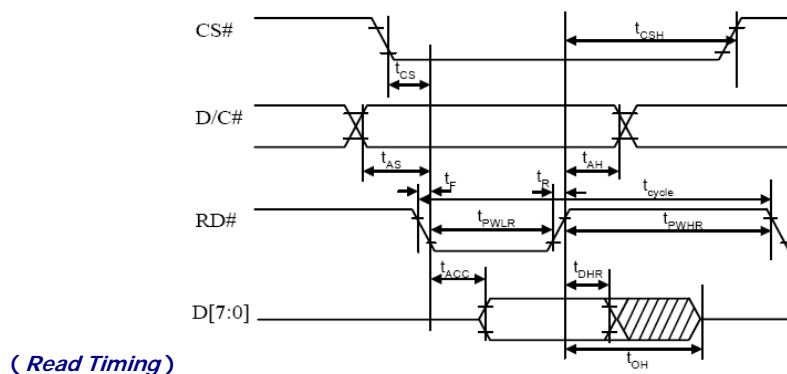


3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	70	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

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* ($V_{DD} - V_{SS} = 1.65V$ to $3.5V$, $T_a = 25^\circ C$)

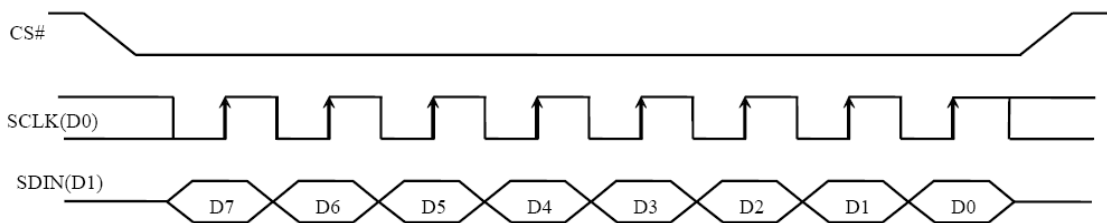
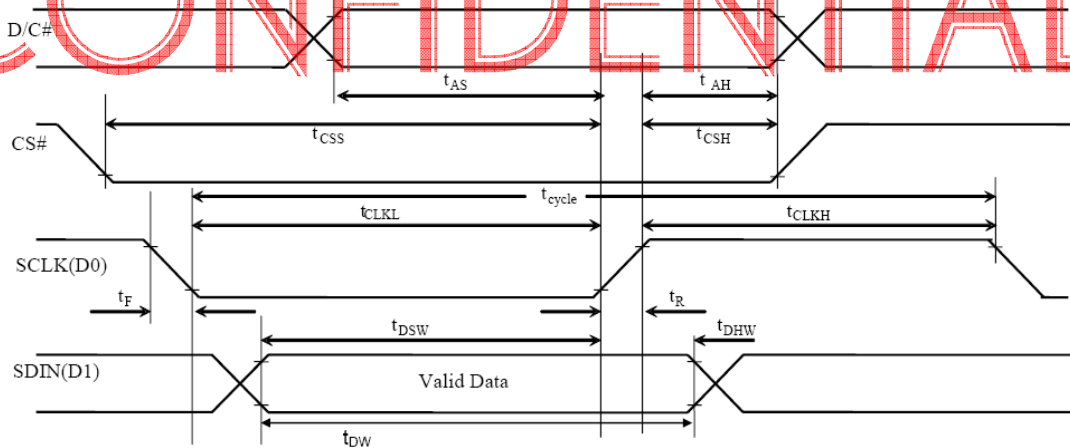


3.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
t_{DW}	Data Write Time	55	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	50	-	ns
t_{CLKH}	Clock High Time	50	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* ($V_{DD} - V_{SS} = 1.65V$ to $3.5V$, $T_a = 25^\circ C$)

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3.3.4 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA _{OUT} " Pin)	0	-	ns
	Data Hold Time (for "SDA _{IN} " Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* ($V_{DD} - V_{SS} = 1.65V$ to $3.5V$, $T_a = 25^\circ C$)

