# Product Specification

(Preliminary)

Part Name: OEL Display Module
Customer Part ID:
WiseChip Part ID: UG-2864ASWPG01
Doc No.: SAS1-090BH-A

| Customer: |
| --- |
| Approved by |



| From: WiseChip Semiconductor Inc. |
| --- |
| Approved by |

**WiseChip Semiconductor Inc.**
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Notes:

1. Please contact WiseChip Semiconductor Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

## *Revised History*

| Part Number | Revision | Revision Content | Revised on |
|---|---|---|---|
| UG-2864ASWPG01 | A | New | June 6, 2012 |

## Contents

# 1. Basic Specifications

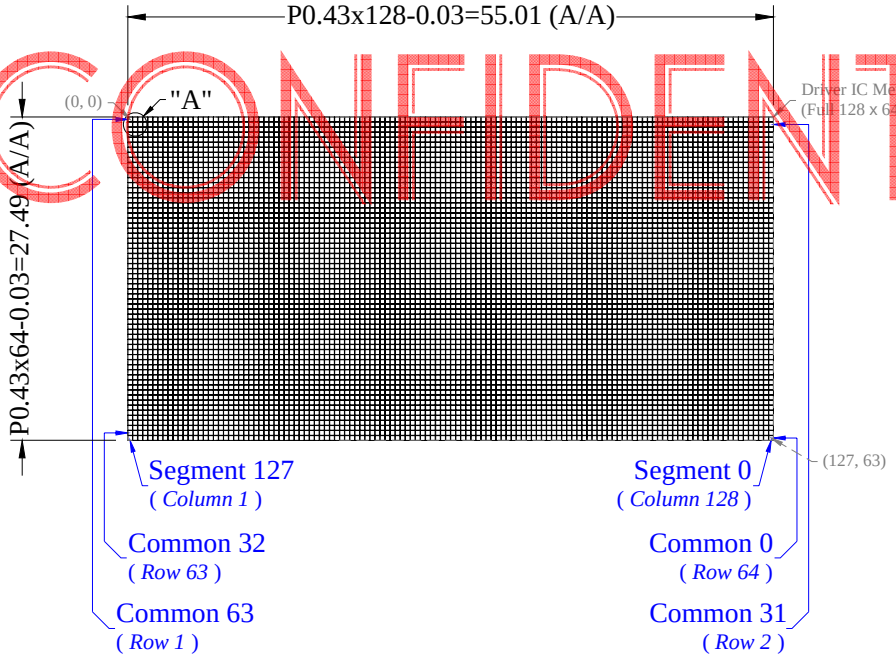
## 1.1 Display Specifications

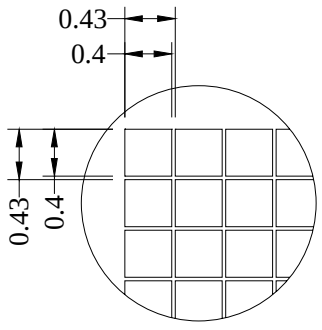
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/64 Duty

## 1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 128 × 64
3) Panel Size: 60.50 × 37.00 × 2.00 (mm)
4) Active Area: 55.01 × 27.49 (mm)
5) Pixel Pitch: 0.43 × 0.43 (mm)
6) Pixel Size: 0.40 × 0.40 (mm)
7) Weight: 8.60 (g)

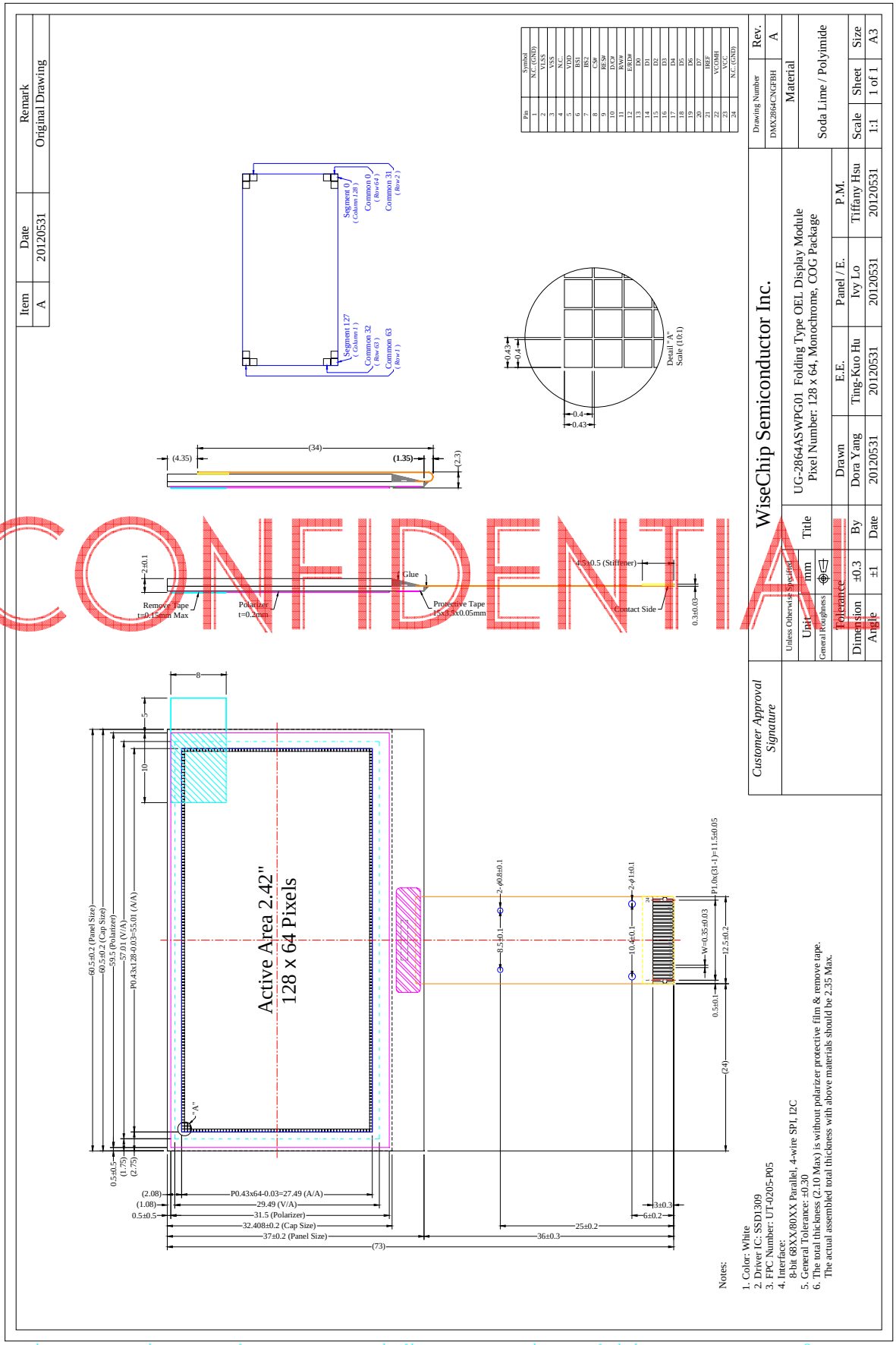
## 1.3 Active Area / Memory Mapping & Pixel Construction




Detail "A"
Scale (10:1)

## 1.4 Mechanical Drawing



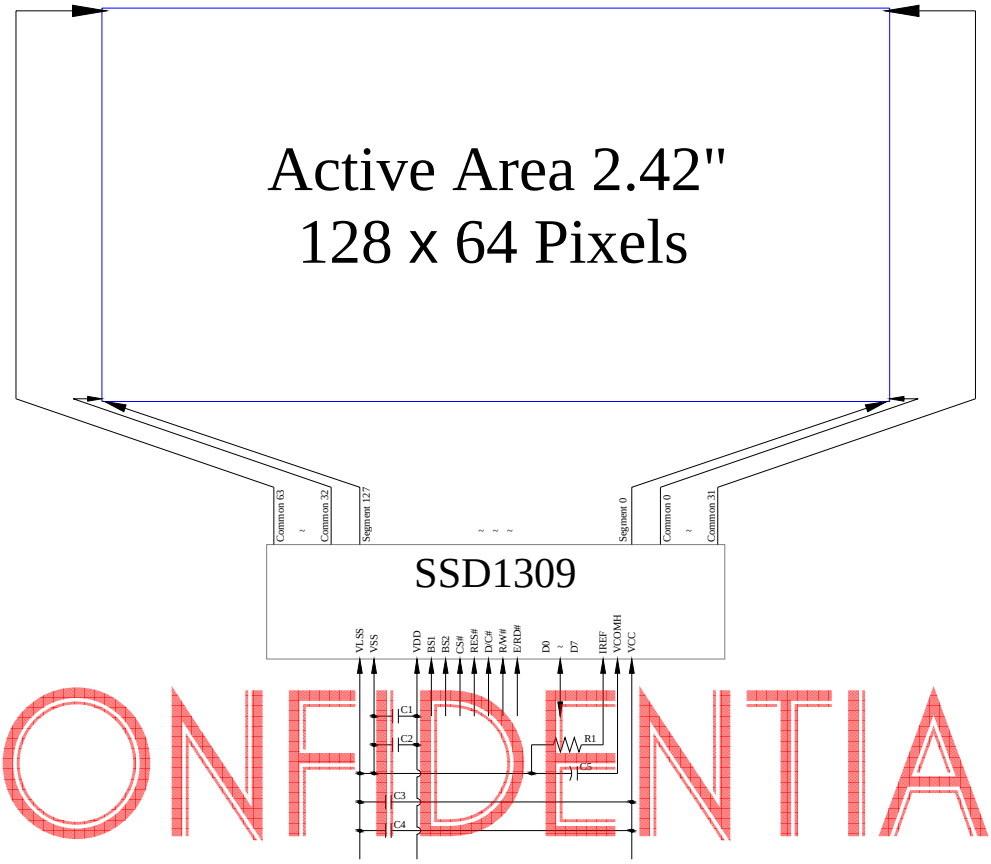
### 1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>5</td><td>VDD</td><td>P</td><td>Power Supply for Logic Circuit<br>This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit<br>This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>23</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel<br>This is the most positive voltage supply pin of the chip. It must be supplied externally.</td></tr>
<tr><td>2</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit<br>This is an analog ground pin. It should be connected to $V_{SS}$ externally.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>21</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment<br>This pin is segment current reference pin. A resistor should be connected between this pin and $V_{SS}$. Set the current at 10μA.</td></tr>
<tr><td>22</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal<br>This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and $V_{SS}$.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>6<br>7</td><td>BS1<br>BS2</td><td>I</td><td>Communicating Protocol Select<br>These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS1</th><th>BS2</th></tr>
<tr><td>$I^2C$</td><td>1</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>9</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver<br>This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>8</td><td>CS#</td><td>I</td><td>Chip Select<br>This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>10</td><td>D/C#</td><td>I</td><td>Data/Command Control<br>This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.<br>When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In $I^2C$ mode, this pin acts as SA0 for slave address selection.<br>For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>12</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.<br>When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.<br>When serial or $I^2C$ mode is selected, this pin must be connected to $V_{SS}$.</td></tr>
<tr><td>11</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.<br>When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.<br>When serial or $I^2C$ mode is selected, this pin must be connected to $V_{SS}$.</td></tr>
</table>

### 1.5 Pin Definition (Continued)

| Pin Number | Symbol | I/O | Function |
|---|---|---|---|
| ***Interface (Continued)*** | | | |
| 13~20 | D0~D7 | I/O | **Host Data Input/Output Bus**<br>These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When $I^2C$ mode is selected, D2, D1 should be tired together and serve as $SDA_{OUT}$, $SDA_{IN}$ in application and D0 is the serial clock input, SCL.<br>Unused pins must be connected to $V_{SS}$ except for D2 in serial mode. |
| ***Reserve*** | | | |
| 4 | N.C. | - | **Reserved Pin**<br>The N.C. pin between function pins is reserved for compatible and flexible design. |
| 1, 24 | N.C. (GND) | - | **Reserved Pin (Supporting Pin)**<br>The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit. |

### 1.6 Block Diagram






MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES#, and CS#

C1, C3: 0.1μF
C2: 4.7μF
C4: 10μF
C5: 4.7μF / 25V Tantalum Capacitor
R1: 910kΩ, R1 = (Voltage at IREF - BGGND) / IREF

## 2. Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply Voltage for Logic | $V_{DD}$ | -0.3 | 4 | V | 1, 2 |
| Supply Voltage for Display | $V_{CC}$ | 0 | 15 | V | 1, 2 |
| Operating Temperature | $T_{OP}$ | -40 | 70 | °C | 3 |
| Storage Temperature | $T_{STG}$ | -40 | 85 | °C | 3 |
| Life Time (80 cd/m$^2$) | | 30,000 | - | hour | 4 |
| Life Time (60 cd/m$^2$) | | 50,000 | - | hour | 4 |

Note 1: All the above voltages are on the basis of "$V_{SS}$ = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: $V_{CC}$ = 13.0V, $T_a$ = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

# 3. Optics & Electrical Characteristics

## 3.1 Optics Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Brightness | $L_{br}$ | Note 5 | 60 | 80 | - | $cd/m^2$ |
| C.I.E. (White) | (x)<br>(y) | C.I.E. 1931 | 0.25<br>0.27 | 0.29<br>0.31 | 0.33<br>0.35 | |
| Dark Room Contrast | CR | | - | >10,000:1 | - | |
| Viewing Angle | | | - | Free | - | degree |

* Optical measurement taken at $V_{DD}$ = 2.8V, $V_{CC}$ = 13.0V.
Software configuration follows Section 4.4 Initialization.

## 3.2 DC Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage for Logic | $V_{DD}$ | | 1.65 | 2.8 | 3.3 | V |
| Supply Voltage for Display | $V_{CC}$ | Note 5 | 12.5 | 13.0 | 13.5 | V |
| High Level Input | $V_{IH}$ | $I_{OUT}$ = 100μA, 3.3MHz | 0.8×$V_{DD}$ | - | $V_{DD}$ | V |
| Low Level Input | $V_{IL}$ | $I_{OUT}$ = 100μA, 3.3MHz | 0 | - | 0.2×$V_{DD}$ | V |
| High Level Output | $V_{OH}$ | $I_{OUT}$ = 100μA, 3.3MHz | 0.9×$V_{DD}$ | - | $V_{DD}$ | V |
| Low Level Output | $V_{OL}$ | $I_{OUT}$ = 100μA, 3.3MHz | 0 | - | 0.1×$V_{DD}$ | V |
| Operating Current for $V_{DD}$ | $I_{DD}$ | | - | 180 | 300 | μA |
| Operating Current for $V_{CC}$ | $I_{CC}$ | Note 6 | - | 18.5 | 23.1 | mA |
| | | Note 7 | - | 27.1 | 33.9 | mA |
| | | Note 8 | - | 42.3 | 52.9 | mA |
| Sleep Mode Current for $V_{DD}$ | $I_{DD, SLEEP}$ | | - | 1 | 5 | μA |
| Sleep Mode Current for $V_{CC}$ | $I_{CC, SLEEP}$ | | - | 2 | 10 | μA |



Note 5: Brightness ($L_{br}$) and Supply Voltage for Display ($V_{CC}$) are subject to the change of the panel characteristics and the customer's request.
Note 6: $V_{DD}$ = 2.8V, $V_{CC}$ = 13.0V, 30% Display Area Turn on.
Note 7: $V_{DD}$ = 2.8V, $V_{CC}$ = 13.0V, 50% Display Area Turn on.
Note 8: $V_{DD}$ = 2.8V, $V_{CC}$ = 13.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

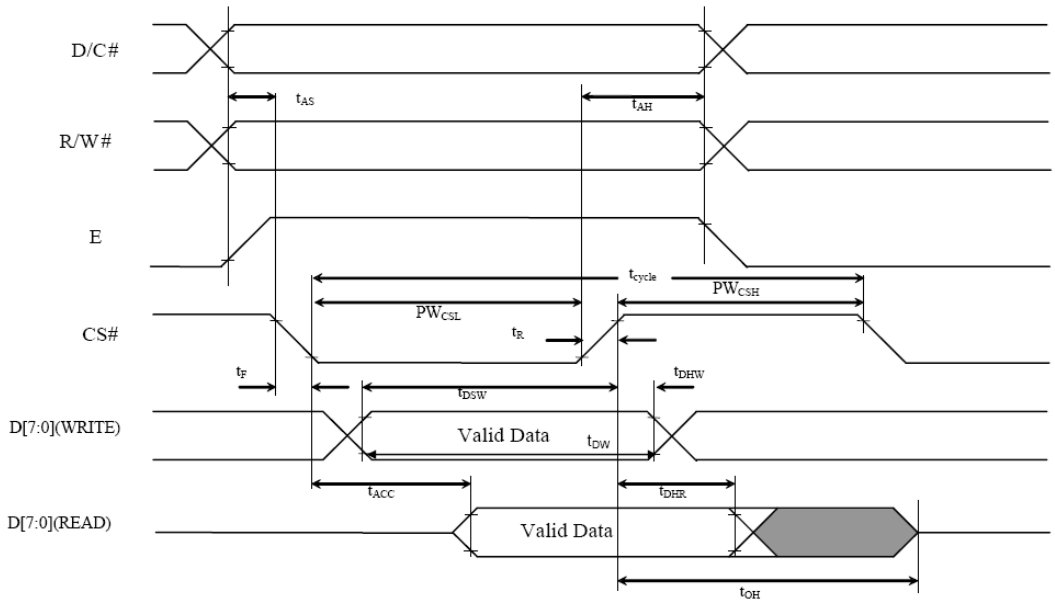
### 3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | ns |
| $t_{AS}$ | Address Setup Time | 20 | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | ns |
| $t_{DW}$ | Data Write Time | 80 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 20 | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | ns |
| $t_{OH}$ | Output Disable Time | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | 140 | ns |
| $PW_{CSL}$ | Chip Select Low Pulse Width (Read) | 120 | - | ns |
| | Chip Select Low Pulse width (Write) | 60 | | |
| $PW_{CSH}$ | Chip Select High Pulse Width (Read) | 60 | - | ns |
| | Chip Select High Pulse Width (Write) | 60 | | |
| $t_R$ | Rise Time | - | 40 | ns |
| $t_F$ | Fall Time | - | 40 | ns |



* ($V_{DD}$ - $V_{SS}$ = 1.65V to 3.3V, $T_a$ = 25°C)

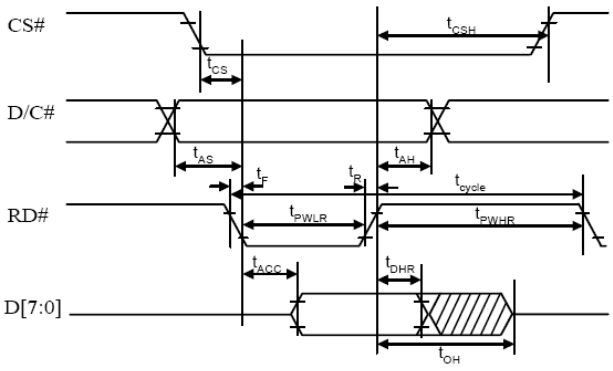


3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

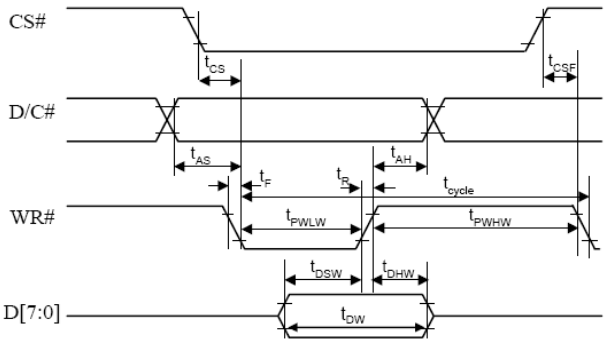
| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | ns |
| $t_{AS}$ | Address Setup Time | 20 | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | ns |
| $t_{DW}$ | Data Write Time | 70 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | ns |
| $t_{OH}$ | Output Disable Time | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | 140 | ns |
| $t_{PWLR}$ | Read Low Time | 120 | - | ns |
| $t_{PWLW}$ | Write Low Time | 60 | - | ns |
| $t_{PWHR}$ | Read High Time | 60 | - | ns |
| $t_{PWHW}$ | Write High Time | 60 | - | ns |
| $t_{CS}$ | Chip Select Setup Time | 0 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time to Read Signal | 0 | - | ns |
| $t_{CSF}$ | Chip Select Hold Time | 20 | - | ns |
| $t_R$ | Rise Time | - | 40 | ns |
| $t_F$ | Fall Time | - | 40 | ns |



* ($V_{DD}$ - $V_{SS}$ = 1.65V to 3.5V, $T_a$ = 25°C)




( ***Read Timing*** )



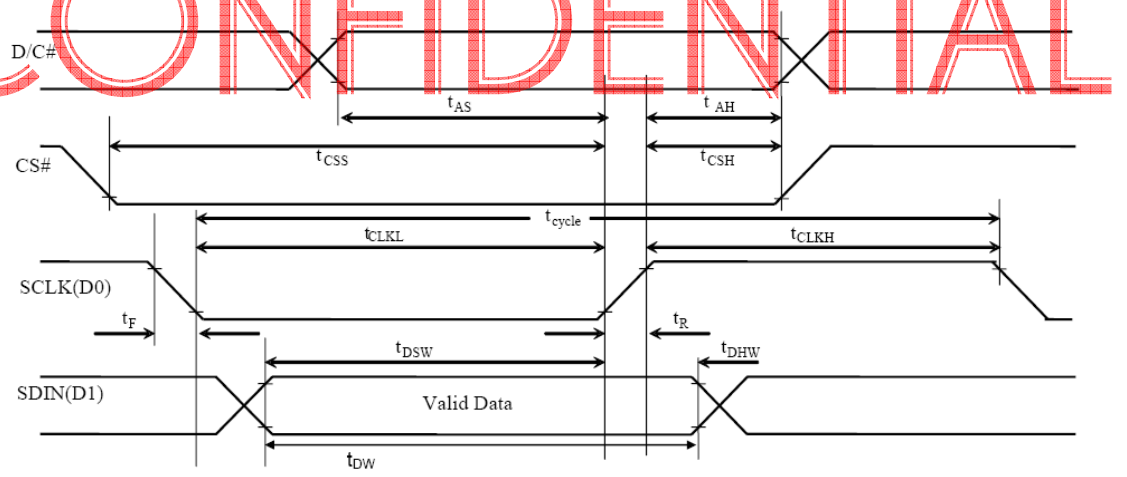

( ***Write Timing*** )

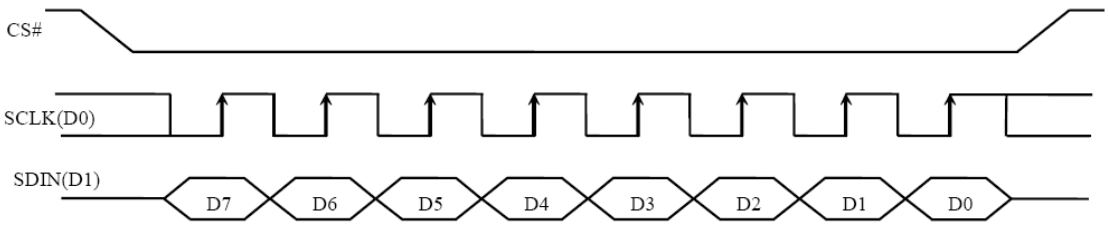
3.3.3 Serial Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | ns |
| $t_{AS}$ | Address Setup Time | 15 | - | ns |
| $t_{AH}$ | Address Hold Time | 15 | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 20 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 50 | - | ns |
| $t_{DW}$ | Data Write Time | 55 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 15 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | ns |
| $t_{CLKL}$ | Clock Low Time | 50 | - | ns |
| $t_{CLKH}$ | Clock High Time | 50 | - | ns |
| $t_R$ | Rise Time | - | 40 | ns |
| $t_F$ | Fall Time | - | 40 | ns |

* ($V_{DD}$ - $V_{SS}$ = 1.65V to 3.5V, $T_a$ = 25°C)





3.3.4 $I^2C$ Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 2.5 | - | μs |
| $t_{HSTART}$ | Start Condition Hold Time | 0.6 | - | μs |
| $t_{HD}$ | Data Hold Time (for "$SDA_{OUT}$" Pin) | 0 | - | ns |
| | Data Hold Time (for "$SDA_{IN}$" Pin) | 300 | | |
| $t_{SD}$ | Data Setup Time | 100 | - | ns |
| $t_{SSTART}$ | Start Condition Setup Time (Only relevant for a repeated Start condition) | 0.6 | - | μs |
| $t_{SSTOP}$ | Stop Condition Setup Time | 0.6 | - | μs |
| $t_R$ | Rise Time for Data and Clock Pin | | 300 | ns |
| $t_F$ | Fall Time for Data and Clock Pin | | 300 | ns |
| $t_{IDLE}$ | Idle Time before a New Transmission can Start | 1.3 | - | μs |

* ($V_{DD}$ - $V_{SS}$ = 1.65V to 3.5V, $T_a$ = 25°C)